

FIGURE 3

FIG. 5 is a schematic diagram of a semiconductor device 500 in accordance with one embodiment of the present invention. The device 500 includes a substrate 502, a gate stack 504, a source region 506, a drain region 508, and a channel region 510. The gate stack 504 is formed over the substrate 502 and defines a gate opening 512. The source region 506 and the drain region 508 are formed on opposite sides of the gate opening 512. The channel region 510 is located within the gate opening 512. The device 500 is configured to operate as a transistor. The source region 506 is connected to a source terminal 514, and the drain region 508 is connected to a drain terminal 516. The gate stack 504 is connected to a gate terminal 518. The device 500 is configured to operate as a transistor. The source region 506 is connected to a source terminal 514, and the drain region 508 is connected to a drain terminal 516. The gate stack 504 is connected to a gate terminal 518.

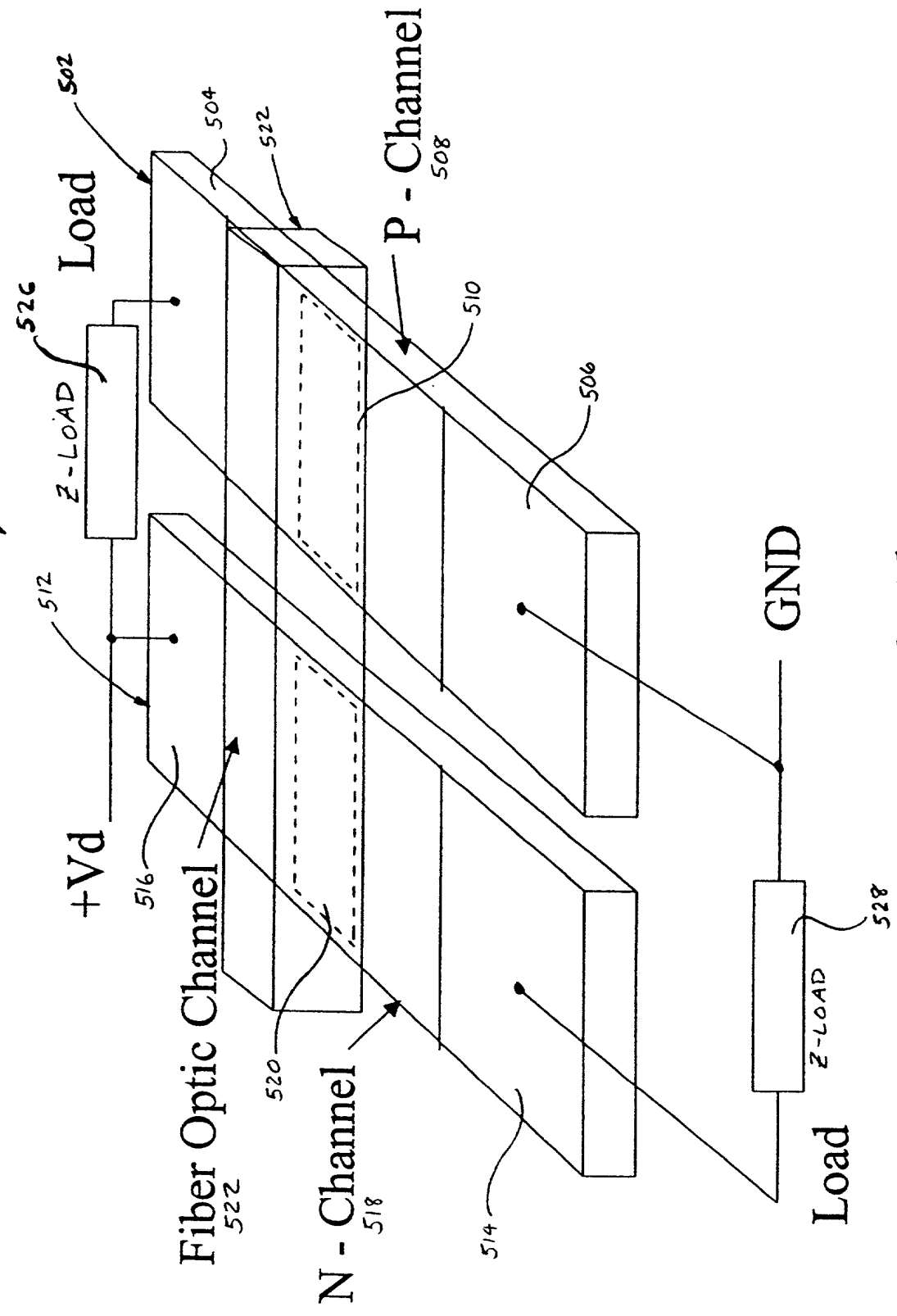


FIGURE 5
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FIG. 6 is a schematic diagram of a device 600 in accordance with the present invention. The device 600 includes a fiber optic channel 610, a P-channel 606, a load 612, and a load 614. The fiber optic channel 610 is connected to the P-channel 606. The P-channel 606 is connected to the load 612. The load 612 is connected to the load 614. The load 614 is connected to GND.

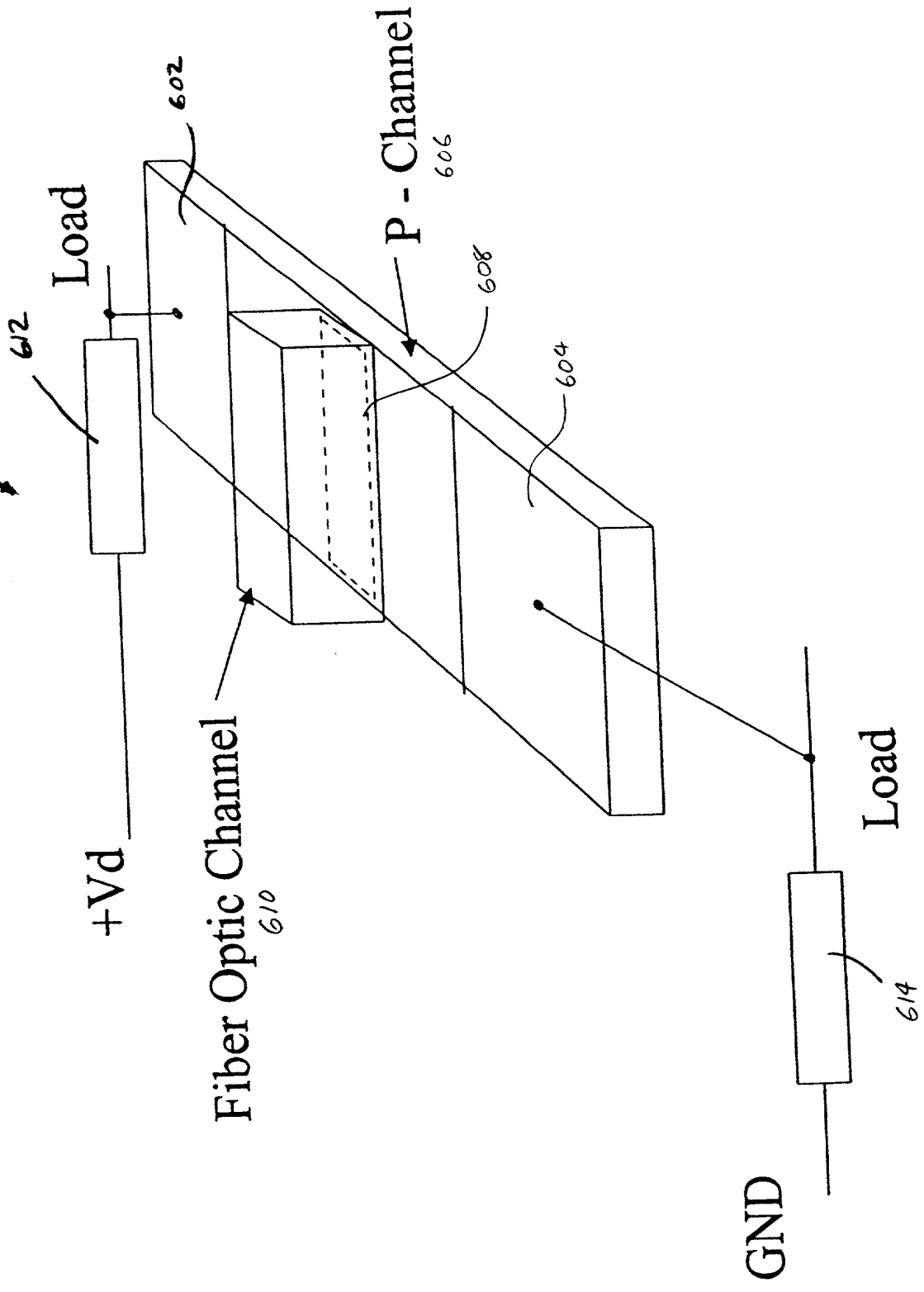


FIGURE 6